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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,566	02/23/2004	Bo Jin	10002.003010 (CD03002)	8641

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OKAMOTO & BENEDICTO, LLP
P.O. BOX 641330
SAN JOSE, CA 95164

EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,566	JIN ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6,12 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,4-6,12 and 16-20* is/are allowed.

6)☒ Claim(s) *21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cha et al (6849928) in view of Nutty et al (6847218).

Regarding claim 21, Cha et al disclose an anti-wafer structure [see Fig. 10] for testing a plurality of dice on a wafer under test, the structure comprising a silicon on insulator (SOI) layer (SOI layer 46); and a plurality of probe dice (pad 42) formed on the SOI layer (46), each probe die in the plurality of probe dice having a pad layout corresponding lo a pad layout of a die on the wafer under test. However, they do not disclose an adapter layer as disclose. Nutty et al disclose [see Figs. 1-3] a silicon on insulator layer (probe card 220), a plurality of probe dice (probe dice 351A-351H) on the SOI layer (220) and an adapter layer (test interface 240) to adapt a pad layout of a probe dice (351A-315H) to another pad layout [not shown]. Further, Nutty et al teach that the addition of adapter layer is advantageous because it increased the throughput and enhance the capability of a test environment by increasing the probe dice so that more test dice may be tested within a given amount of time. It would have been obvious to a person having

ordinary skill in the art at the time the invention was made to modify the apparatus of Cha et al by adding adapter layer as taught by Nutty et al in order to increase the throughput and enhance the capability of a test environment during testing.

Regarding claim 22, Cha et al disclose a plurality of holes (holes 34 and 36) extending through the SOI layer (46) and the plurality of probe dice (42), the holes (34 and 36) corresponding to pads (42) on the probe dice.

Regarding claim 23, Nutty et al disclose [see Figs. 8A-8E] a silicon on insulator layer (220), a plurality of probe dice (831) on the SOI layer (220) and a plurality of holes (shown not number) extending through the plurality of probe dice (220) wherein the holes are filed with interconnect lines (interconnect lines 855). Further, Kurita teaches that the addition of interconnect lines inside holes is advantageous because cracks that are caused in a solder ball connection can significantly be reduced. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Cha et al by adding interconnect lines in holes extending through probe dice as taught by Nutty et al in order to significantly reduced cracks that are caused in a solder ball connection.

Regarding claim 24, Nutty et al disclose the interconnect lines (855) are coupled to pads (821) of the wafer under test (851).

Regarding claim 25, Cha et al disclose a number of the probe dice (42) equals a number of dice on the wafer under test.

Regarding claim 26, Cha et al disclose the SOI layer (46) comprises an oxide layer (oxide layer 14).

Conclusion

4. Claims 1, 4-6, 12, 16-20 are allowed.

5. The following is a statement of reasons for the indication of allowable subject matter: regarding claims 1 and 12, the reason for the allowance of the claims is presented in the "Remarks" section of the applicants' amendment filed on Nov. 15, 2005. Since claims 4-6 depend from claim 1 and claims 16-20 depend from claim 12, they also would have allowable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (517) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMH
February 6, 2006

Jermele M. Hollington
Primary Examiner
Art Unit 2829